Summary

This fully revised and popular book is now up-to-date and even more comprehensive than before. The Indispensable PC Hardware Book 4/e will be 'indispensable' to anyone who wants to know more about the inner workings of a personal computer: from programmers who want access to hardware components; professionals and home-users who wants to or has to understand the structure and functioning of a personal computer; to users who want to up-grade their PC’s, and dealers who wish to advise their customers--this book will provide the solution to all your hardware questions. Even beginners should not shy away as this book begins with an easy introduction to the subject area.

Key highlights:

- CPU's from the 8086/8088 to the Pentium III and Athlon
- Real, protected and virtual models
- Windows and plug&play devices
- CPU Clones from all major manufacturers
- Chipsets and support chips
- Timers, interrupts and DMA
- I/O programming and PCI bus programming
- AGP variants and graphic systems
- Universal serial bus
- Local storage from the diskette to DVD
- Memory systems, SDRAM, EDO, flas, RAM bus, and modules
- Extensive glossary which explains most of the terms and concepts related to personal computer hardware.
- Appendices brimming with practical advice, especially for programmers.

Author Bio

Hans-Peter Messmer is a physicist who for many years has worked as a freelance consultant in the hardware and software industries. He owns a software house in Quito, Ecuador.

Table of Contents

I. BASICS.

1. The Main Components of a PC.
   - The Computer and Peripherals.
   - Inside the Personal Computer.
   - How to Open the Case.
   - Protecting Yourself Against Electric Shocks.
II. THE PC’S MICROPROCESSORS.

2. Introduction to Microprocessor Technology.
   The Field-effect Transistor.
   Basics of Machine-related Information Representation.
   Decimal and Binary Systems.
   ASCII Code.
   Negative Integers and Two's Complement.
   Hexadecimal Numbers.
   BCD Numbers.
   Little Endian Format and Intel Notation.

   Logic Gates.
   Basic Logical Elements.
   CMOS Inverters as Low-power Components.
   An Example: 1-bit Adder.

   The CPU as the Core of all Computers.

3. Everything Began with the Ancestor 8086.
   Pins and Signals in the 8086.
   8086 operating modes and the 8288 bus controller.
   8086 real mode.
   Accessing the memory.
   Word boundaries.
   Accessing the I/O address space.
   8086 reset.
   The 8088.
   The 80186/88.

4. Downwards compatibility — the 80286.
   Pins and signals in the 80286.
   The 80286 registers.
   80286 protected mode.
   80286 memory management registers.
   80286 segment descriptors.
   80286 segment and access types.
   Multitasking, 80286 TSS, and the 80286 task gate.
   80286 Protection for I/O address space.

   80286 Bus cycles and pipelining.
   Word boundaries.
   80286 reset.

5. Introduction to the world of 32-bit computing — the 80386.
   Pins and signals in the 80386.
   Access to physical memory and the ports.
   Bus cycle for read access.
   Bus cycle for write access.
   Wait states.
   Address pipelining or pipelined addressing.
Double word boundary.
Special cycles.
Data bus and write data duplication.
I/O address space and the peripherals.
I/O addressing.
I/O cycles.

Registers.
Registers overview.
Segmenting.
General purpose and segment registers.
Flags.
Control and memory management registers.

6. Programming and operating types.
Code segment and instruction counter.
Stack segment and stack pointer.
Data segment DS and addressing.
Addressing types and instruction coding.
  Programming at processor level: mnemonics and the assembler.
  Addressing types.
  Instruction coding.
  Loading instructions and prefetching.

Real mode, high memory area, and HIMEM.SYS.
Interrupts and exceptions.
  Software interrupts.
  Hardware interrupts.
  Exceptions.

Protected Mode.
  Segment selectors, segment descriptors, and privilege levels.
  Global and local descriptor tables.
  Switching into protected mode.
  Memory addressing in protected mode.
  Control transfer and call gates.
  Interrupt descriptor table.
  Multitasking, TSS, and task gates.
  Protecting the I/O address space.
  Protected mode exceptions and protection mechanisms.

Paging.
  Logical, linear, physical addressing, and paging.
  Page Directory, page tables, and page frames.
  Test registers TR6 and TR7.

Virtual 8086 mode.
  Virtual machines and virtual 8086 monitors.
  Addresses in virtual 8086 mode.
  Entering and leaving virtual 8086 mode.
  Tasks in virtual 8086 mode.

7. Quick buffering: caching.
Cache principle and cache strategies.
Cache organization and associative memory (CAM).
Cache hit determination and optimum cache size.
Replacement strategies.
On-chip and second-level caches.
Cache consistency and the MESI protocol.
  The four MESI states.
  MESI state transitions.
  L2 cache sub-systems and the MESI cache consistency protocol.

Pipelined burst cache.

8. All in one—the i486.
  Pins and signals of the i486.
  Internal structure of the i486.
  RISC or CISC.
  Microcoding.
  Back to basics.
RISC characteristics at hardware level.
RISC characteristics at software level.

The pipeline.
The on-chip cache.
Differences and common attributes of i486 and 80386/80387.
  Differences in register structures.
  Differences in memory management.
i486 reset.
i486 real mode.
i486 protected mode.
i486 virtual 8086 mode.
Integer core and floating-point unit.
FPU exceptions.
Translation lookaside buffer (TLB).

The i486 bus.
  Burst cycles.
  Special cycles.
  Invalidation cycles.

Test functions.
  BIST internal self-test.
  Testing the TLB.
  Testing the on-chip cache.
  Tristate test mode.
  JTAG boundary scan test.

The i486's address space.


Mathematical coprocessors.
  Numbers game—The representation of floating-point numbers.
  The standard—IEEE formats.
  Functionality and structure.
  80387 exceptions.
  Protected mode and memory images of instruction and data pointers.

386 processor derivatives and clones.
  Cutting down: the SX variants of the processors.
  386 CPUs from other manufacturers.
  Cyrix 386 processors (486xLC).
  Overview of 386 and 486 CPUs.

486 Processor derivatives and clones.
  i486SX and i487SX.
  i486SX upgrade: the i487SX.
  i486DX2 processors with internal frequency doubling.
  The i486DX4.
  Other 486 CPUs.

10. The Pentium.

Pins and signals.
The internal structure of the Pentium.
  The integer pipelines u and v.
  Instruction pairing in the integer pipelines.
  The floating-point pipeline.
  Serializing instruction execution.
  Dynamic branching prediction and branch prediction logic.
  The Pentium on-chip caches.

Pentium compatibility.
  Extensions to the Pentium registers.
  Model-specific registers.
  Feature control register TR12.
  Pentium real mode.
  Pentium protected mode.
  Pentium virtual 8086 mode.
  Paging on the Pentium.
  Debug extensions.
  Pentium reset, Pentium init, and self-test.
  CPU identification with CPUID.
New Pentium exceptions.

The Pentium bus.
- Single transfer cycles.
- Burst cycles.
- Pentium address pipelining.
- Special bus cycles.
- Query cycles and internal snooping.
- Pentium internal bus buffers.

Pentium system management mode.
- SMM RAM structure.
- Program execution in system management mode.
- Returning from system management mode.

Code optimization.
- Simple straightforward optimization.
- Optimization with performance monitoring.

Pentium test functions.
- Pentium JTAG boundary scan test.
- Detecting internal errors.
- Detecting bus faults.
- Execution tracing.
- Hardware debug support and probe mode.
- Machine check exception.

Pentium I/O address space.
- Dual processing.
  - General dual-processing structure with two Pentiums.
  - Bus arbitration.
  - Cache consistency.
  - On-chip APICs.

A third-generation Pentium—MMX.
- Pins and signals.

MMX technology.
- SIMD and MMX data types.
- MMX registers.
- MMX instructions.

11. Pentium-compatible microprocessors.

CPUs from Cyrix.
- The Cyrix 6x86.
- The Cyrix 6x86MX.

CPUs from AMD.
- The K5—5K86.
- The AMD K6.
- AMD K6 II and AMD K6 III with Super Socket 7.

IDT WinChip C6.
- CPU Overview and settings.


Pins and signals.
- Internal structure.
  - Functional units of the Pentium Pro.
  - Instruction pool and micro-ops.
  - L1 and L2 caches.

Pentium Pro features.
- Instructions.
- Control functions in CR4.
- The 36-bit address bus.
- Global pages.

Model-specific registers.
- Memory type range registers (MTTR).
- Configuration registers.
- Machine check architecture.
Performance monitoring.
Model-specific registers for debug support.

Reset and power-on configuration.
The Pentium Pro’s bus.
Bus phases.
Bus arbitration.
Deferred transactions.
Bus pipelining and Pentium Pro Bursts.

Multiprocessing.
CPUID.

Pentium II.
Pins and signals.
The Pentium II bus (GTL+).

The Celeron.
Pins and signals.
The Celeron for the Socket 370.

The Pentium III.
Family members.
Pentium III for the Socket 370.
Pins and signals.

The Celeron III.
The Cyrix III.
CPU Settings.

The bus protocol.
Pins and signals.
Internal structure.
Athlons for Socket A.
Pins and signals.

III. MEMORY, CHIPSETS, AND SUPPORT CHIPS.

15. Memory chips: the computer’s memory.
Small and cheap: DRAM.
Structure and operation principle.
Reading and writing data.
Semiconductor layer structures.
Refreshing the DRAM.
DRAM chip organization.
DRAM chip operating modes.

Memory modules.
Parity.
DIM modules.
Synchronous dynamic RAM: SDRAM and DDR RAM.
Synchronous graphic RAM: SGRAM.
RAMBus.

Fast and expensive: SRAM.
The flip-flop.
Accessing SRAM memory cells.
Typical SRAM.

Long-term memory: ROMs, EPROMs, and other memory.
ROM.
EPROM.
EEPROM.
Flash memory.

486 PCI chipset.
Intel Pentium chipsets for Socket 7.
Alternative Socket 7 chipsets.
Pentium Pro and Pentium II chipsets.
Pentium II, Pentium III, and Celeron chipsets.
  Intel 810 chipset: Whitney.
  Intel 820 chipset: Camino.
  Intel 840 chipset: Carmel.
  Intel 815 chipset: Solano.
Chipsets from different manufacturers.

Athlon chipsets.
A brief overview.

17. Hardware interrupts and DMA.
   Hardware interrupts and the programmable interrupt controller (PIC).
   Interrupt-driven data exchange and polling.
   Pins and signals of the 8259A.
   Internal structure and interrupt acknowledge sequence.
   Cascading.
   Initialization and programming.
   Masking NMIs.
   Multiprocessor interrupt subsystem.

Direct memory access with peripherals and memory.
    Standard 8237A DMA chip.

18. CMOS RAM and realtime clock.
    Structure and programming.
    Access via BIOS.
    Access via the address and data register.

19. The timer and other peripheral chips.
    The programmable interval timer.
    Pins and signals.
    Programming the 8253/8254.
    System clock.

Motherboard peripheral units.
  Super I/O controller.
  Supervisory chips.

IV. PERSONAL COMPUTER ARCHITECTURES AND BUS SYSTEMS.

20. The 8-bit PC/XT architecture.
    The components and how they work together.
    DMA architecture.
    8-bit channels.
    Memory refresh.
    Memory to memory transfer.

I/O channel and bus slots.

21. 16-bit architecture.
    The components and how they work together.
    DMA architecture.
    8-bit and 16-bit channels.
    Memory refresh.
    Memory to memory transfers.

I/O channel and bus slots.
AT bus frequencies and the ISA bus.

22. EISA architecture.
    EISA bus structure.
    Bus arbitration.
    DMA architecture.
    Interrupt subsystem.
    EISA timer and failsafe timer.
    I/O address space.
    CMOS-RAM.
23. Microchannel.
- MCA bus structure.
- Bus arbitration.
- Memory system.
- DMA.
- Interrupts.
- MCA timer and failsafe timer.
- I/O ports and I/O address space.
- MCA adapters and automatic configuration.
- MCA slots.
- MCA signals.

24. The VESA local bus (VLB).
- VLB bus structure.
- Bus cycles.
  - Burst cycles.
  - 16-bit transfers.
  - 64-bit transfers.
  - Support for write-back caches.
- Bus arbitration.
- DMA and interrupts.
- I/O address space.
- VLB slots.
- VLB signals.
  - Standard 32-bit section.
  - 64-bit expansion.

25. The PCI bus.
- PCI bus structure.
- Bus cycles.
- Bus arbitration.
- DMA and bus mastering.
  - Scatter gather bus mastering.
- Interrupts.
- I/O address space.
- Configuration address space.
- PCI slots.
- PCI signals.
  - Standard 32-bit section.
  - 64-bit expansion.
- PCI-specific BIOS routines.
  - The interface to the BIOS.
  - The function pci_bios_present.
  - The function find_pci_device.
  - The function find_pci_class_code.
  - The function read_configuration_area.
  - A universal PCI unit.

26. ISA Plug & Play.
- What does Plug & Play mean here?
- The configuration mechanism.
  - Linear feedback shift register.
  - Isolation protocol.
- The ISA Plug & Play register.
- How to access ISA Plug & Play devices.

27. Accelerated graphics port and 3-D graphics.
- AGP structure.
- AGP signals.
- AGP slots.
- AGP transfers.
- 3-D graphics with the AGP.
  - How the CPU and 3-D chips work together.
V. MASS STORAGE AND ITS INTERFACES.

28. Floppies and floppy drives.
   Ferromagnetism and induction: the basis of magnetic data recording.
   Diamagnetism and paramagnetism.
   Ferromagnetism.
   Induction.

   Floppies and floppy drives: their structure and how they work.
   Physical organization of floppies.
   Logical organization of floppies and hard disks under DOS.
   Logical sectors.
   Partitions.
   The boot sector.
   The root directory.
   Subdirectories.
   The file allocation table (FAT).

   Integration: controller and disk drives.
   Do diskette drives have a terminating resistor?
   The emergence of ghost directories.

   Recording formats and CRC.
   Sector layout.
   FM and MFM.
   CRC: nothing can hide from me.
   For the seriously interested: some amazing features of CRC code.

   Programming floppy drives.
   Access via BIOS interrupt INT 13h.

   The disk drive controller and its registers.
   Floppy controller registers.
   Commands and command phases.
   Specifying drive parameters.
   Error recovery strategy.

29. Hard disks.
   Structure and functionality of hard disks.
   Disks.
   Heads.
   Actuators with a stepper or linear motor.
   Air filtering and ventilation.
   Interleaving.
   A few notes on hard disk data.

   Recording formats.
   MFM and RLL.
   Translating and zone recording.
   Using FORMAT for high-level formatting of hard disks.
   Low-level formatting and bad-sector mapping.

   Hard disk interfaces.
   ST412/506 interfaces and the connection between the drive and controller.
   The ESDI interface.
   Drives with IDE, AT bus, or ATA interface.
   Enhanced IDE.

SCSI.
   SCSI bus and connection to the PC.
   Bus phases and messages.
   Programming and command phases.
   The different SCSI standards.
   SCSI-I and CCS.
   SCSI-II.
   SCSI-III.
   Fast SCSI.
31. Optical mass storage.
- CD-ROM.
- ATAPI.
- CD-R and CD-R/W.
- CD-RW and phase change technology.
- Magneto-optical drives.
- Digital versatile disk.
- DVD drives.
- Video and regional codes.

VI. EXTERNAL AND PERIPHERAL DEVICES.

32. The parallel port.
- Primary task: printing.
- Printing via BIOS interrupt INT 1h.
- Structure, functionality, and connecting to printers.
- Programming the registers directly.
- General assignment and usage.
- The improved parallel port: IEEE-124.

33. The serial port.
- Serial and asynchronous data transfer.
- RS-232C interface.
- Connection to printers and the nullmodem.
- Access via DOS.
- Access via the BIOS.
- UARTS 8250/16450/16550.

34. The keyboard, mouse, and joystick.
- The keyboard.
- Structure and functionality of keyboards.
- Scan codes: a keyboard map.
- Keyboard access via DOS.
- Keyboard access via the BIOS.
- Programming the keyboard directly via ports.
- The mouse.
- Structure and functionality.
- Mouse drivers and the mouse interface.
- Programming the mouse.
- The PS/2 mouse.

35. Universal serial bus.
- 100BaseVG-Any-LAN.
- Asynchronous transfer mode.
- Ethernet.
- Thick Ethernet.
- CheaperNet or Thin Ethernet.
- Ethernet with twisted-pair cable.
- Fast Ethernet and Gigabit Ethernet.
- Token Ring.
- FDDI.
- Repeater, hubs, switches, and gateways.

Repeaters.
Hubs.
Switches.
Bridges.
Displaying images on a monitor and the general structure of graphics adapters.
Screen display and graphics control chip.
The 6845 video controller.
Character generation in text mode.
Creating graphics and free graphics in graphics mode.
General points about the organization and structure of video RAM.

The main adapter types and their characteristics.
MDA: all very gray.
CGA: let there be color!
Hercules: the non-standard standard.
EGA: more colors and a higher resolution.
VGA: the card of many colors.
VESA modes: high-resolution standards.
Windows accelerators.
TIGA.

How to access graphics adapters.
Access via the BIOS.
Graphics routines in standard BIOS.
EGA and VGA BIOS.
VESA BIOS.
Access to image memory.

A graphic accelerator: Trio64V.
Pins and signals.
Structure of a Trio64V+graphics card.
The streams processor.

APPENDICES.

Appendix A. ASCII and scan codes.
ASCII codes table.
Scan codes (US).
Scan codes (UK).

Appendix B. Interrupts and DMA.
Hardware interrupts.
Software interrupts.
DMA.

Appendix C. Accessing ports.
The printer port.
DOS functions.
BIOS functions.
Printer status byte.

Appendix C. The serial port.
DOS functions.
BIOS functions.
Transmit status.
Modem status.
Parameter byte.
Modem control register.

Appendix D. Access to keyboard and mouse.
The keyboard.
DOS functions.
BIOS interrupt INT 16h.
BIOS interrupt INT 15h.
First shift status byte.
Second shift status byte.
Mouse interrupt 33h.
Functions of INT 33h.
Button byte.
PS/2 Mouse Support via BIOS Interrupt INT 15h, Function c2h.
Subfunctions of INT 15h, Function c2h.
Status byte.
Mouse packet on the stack.

Appendix E. The commands of the (E)IDE interface (ATA).
Commands in detail.

Appendix F. SCSI Commands.
Commands list.
Commands for disk drives.
6-byte commands.
10-byte commands.
Status keys.
Additional status codes.

SCSI commands for other device classes (tape drives to communications devices).
Commands for tape drives (streamers, code 01).
Commands for printers (code 02).
Commands for processors (code 03).
Commands for WORM (Write-once) drives (code 04).

Commands for CD/DVD-ROM drives (code 05).
Commands for scanners (code 06).
Commands for optical memory (code 07).
Commands for medium change devices (code 08).
Commands for communications devices (code 09).
ASPI programming interface.
ASPI functions.
SCSI request block.
ASPI functions.

Appendix G. Glossary.
Index. 0201596164T10312001